

receiving an input signal at an input of the input/output device; and

modifying the input signal based on the selected logic standard; wherein at least one of the multiple logic standards is a differential logic standard.]

75. (Cancelled) [The method of claim 74, wherein the modifying further comprises modifying the input signal to comply with a logic standard selected from the group consisting of TTL, CMOS, open drain logic, GTL, terminated HSTL, and non-terminated HSTL.]

In the Drawings

Applicant respectfully requests approval for the following amendment to FIG. 4 that is indicated in red ink on the attached photocopy of FIG. 4. The proposed amendment merely corrects an error to the drawing correction (FIG. 4) filed on March 4, 2003. The error is that a solid dot indicating that 422, 424, and 412 are connected is missing. The proposed amendment inserts the solid dot indicating that 422, 424, and 412 are connected. No new matter would be added as a result of this proposed amendment. Moreover, in compliance with 37 C.F.R § 1.173(b)(3), applicants also provide a formal drawing